UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,381	06/29/2004	Masatake Nakano	120164	9028

25944 7590 03/13/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,381	NAKANO, MASATAKE	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 7-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 7-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *12/12/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 12/16/05. Currently, claims 722 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inazuki et al., US Patent 6,362,076 in view of Able et al., US Patent 6,544,656.

Inazuki discloses the semiconductor method substantially as claimed. See figures 1-4, and corresponding text, where Inazuki shows, pertaining to claim 7, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **3** on at least one of a bond wafer **2** made of silicon single crystal to form an SOI layer and a base wafer **1** made of silicon single crystal to be a support substrate (figure 1; col. 4, lines 45-56), bonding each main surface of the bond wafer and the base wafer via the insulator film (figure 1; col. 4, lines 64-67; col. 5, lines 1-3), and making the bond wafer bonded to the base wafer thinner, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, and FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the base wafer (figure 1; col. 5, lines 17-27; col. 6, lines 39-45, epitaxial or FZ wafers).

Inazuki shows, pertaining to claim 8, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **3** on at least one of a bond wafer **2** made of silicon single crystal to form an SOI layer and a base wafer **1** made of silicon single crystal to be an support substrate (figure 1; col. 4, lines 45-56), forming a micro bubble layer in the bond wafer by implanting gas ions from a main surface of the bond wafer (figure 1; col. 4, lines 57-63), bonding the ion-implanted main surface of the bond wafer to a main surface of the base wafer via the insulator film (figure 1; col. 4, lines 64-67; col. 5, lines 1-3) , and delaminating the bonded wafer at the micro bubble layers as a border, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the base wafer (figure 1; col. 5, lines 4-35; col. 6, lines 39-45 epitaxial and FZ wafers).

Inazuki shows, pertaining to claims 9 and 10, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the bond wafer (col. 6, lines 39-45).

Inazuki shows, pertaining to claims 11 and 12, wherein the SOI layer to be formed has a thickness of 0.3 μm or less. In addition, Inazuki teaches, pertaining to claims 13-18, wherein the SOI layer to be formed has a thickness of 0.3 μm or less (col. 4, lines 11-15). Also, Inazuki teaches, pertaining to claims 19-22, an SOI wafer produced by the method according to claims 7-10 (figure 1; col. 5, lines 36-41).

However, Inazuki fails to show, pertaining to claims 7 and 8, wherein the base wafer is one of silicon wafer selected from a group consisting an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer.

Abe teaches, a similar method of manufacturing method that includes the use of a FZ wafer as a base wafer (col. 11, lines 55-60).

It would have been obvious to one of ordinary skill in the art to substitute, wherein the base wafer is one of silicon wafer selected from a group consisting an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer, in the method of Inazuki, pertaining to claims 7 and 8, according to the teachings of Abe, with the motivation that, by using a FZ wafer, the advantage would be create an SOI wafer with high resistivity against further semiconductor manufacturing processing.

Response to Arguments

Applicant's arguments, see Remarks, filed 12/16/05, with respect to the rejection(s) of claim(s) 7-22 under 102(a/e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Inazuki et al., US Patent 6,362,076 in view of Able et al., US Patent 6,544,656.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
March 5, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER